

What is claimed is:

1. A multi-phase clock generation circuit

2 comprising:

3 reference clock signal generation means for
4 generating 2^n (n is a positive integer) reference clock
5 signals having the same frequency, the plurality of
6 reference clock signals having different phases;

7 first frequency division means for
8 frequency-dividing one of the plurality of reference
9 clock signals from said reference clock signal
10 generation means by 2 to generate first and second clock
11 signals 180° out of phase with each other on the basis
12 of frequency division outputs;

13 first clock selection means for selecting one
14 of each of the first and second clock signals from said
15 first frequency division means and a corresponding
16 reference clock signal and outputting the selected
17 signals as first and second clock pulses;

18 second to nth frequency division means each of
19 which frequency-divides a clock pulse from said first
20 clock selection means to generate $(2^m - 1)$ th to
21 $(2^{m+1} - 2)$ th (m is a positive integer of not less than 2)
22 clock signals 180° out of phase with each other on the
23 basis of frequency division outputs;

24 second to nth clock selection means each of
25 which selects one of each of the clock signals from said

26 second to nth frequency division means and a
27 corresponding one of the reference clock signals to
28 output the selected signals as $(2^m - 1)$ th to $(2^{m+1} - 2)$ th
29 clock pulses; and
30 clock selection control means for controlling
31 said first to nth clock selection means in accordance
32 with a set frequency division ratio.

2. A circuit according to claim 1, wherein said
2 clock selection control means comprises frequency
3 division number setting means for setting a frequency
4 division number for a clock signal output from
5 predetermined clock selection means.

3. A circuit according to claim 1, wherein
2 said circuit further comprises first-stage
3 frequency division means for generating a clock signal
4 from an arbitrary one of the plurality of reference
5 clock signals, and
6 said first frequency division means generates
7 first and second clock signals 180° out of phase with
8 each other by frequency-dividing the generated clock
9 signal by 2.

4. A circuit according to claim 1, wherein
2 each of said first to nth frequency division
3 means comprises D flip-flop circuits and inverters.

5. A circuit according to claim 4, wherein an
2 output terminal of a predetermined D flip-flop circuit
3 of the D flip-flop circuits is connected to an input
4 terminal of another D flip-flop circuit forming said
5 frequency division means.

6. A circuit according to claim 5, wherein a
2 clock signal output from a predetermined D flip-flop
3 circuit and a clock signal input to another D flip-flop
4 circuit have the same timing.

7. A circuit according to claim 1, further
2 comprising clock shut-off means for shutting off at
3 least some of clocks input to said first to nth clock
4 selection means which are not in use.

8. A circuit according to claim 3, wherein said
2 first-stage frequency division means comprises
3 a D flip-flop circuit, and
4 an inverter.

9. A circuit according to claim 1, wherein said
2 reference clock signal generation means comprises a PLL
3 circuit.

10. A circuit according to claim 1, further

2 comprising reference clock signal selection means for
3 selecting an arbitrary reference clock signal of the
4 plurality of reference clock signals which is input to
5 said first frequency division means.

11. A circuit according to claim 3, further
2 comprising reference clock signal selection means for
3 selecting an arbitrary reference clock signal of the
4 plurality of reference clock signals which is input to
5 said first-stage frequency division means.

12. A multi-phase clock generation circuit
2 comprising:
3 reference clock signal generation means for
4 generating 2^n (n is a positive integer) reference clock
5 signals having the same frequency, the plurality of
6 reference clock signals having different phases;
7 first to n th frequency division means each of
8 which frequency-divides one of an input reference clock
9 signal and a clock by 2 to generate $(2^p - 1)$ th to
10 $(2^{p+1} - 2)$ th (p is a positive integer of not less than 1)
11 clock signals 180° out of phase with each other on the
12 basis of frequency division outputs;
13 first to n th clock selection means each of
14 which selects one of each of clocks signal from said
15 first to n th frequency division means and a
16 corresponding one of the reference clock signals to .

17 output the selected signals as $(2^p - 1)$ th to $(2^{p+1} - 2)$ th
18 clock pulses; and
19 clock selection control means for controlling
20 said first to nth clock selection means in accordance
21 with a set frequency division ratio.